# SEMICONDUCTOR DEVICE AND METHOD

## Field of the Invention

The present invention relates in general to semiconductor devices, and more particularly to transistors fabricated in high density integrated circuits.

## Background of the Invention

There currently is a need for integrated circuits with higher density and increased functionality. To meet this need, it is necessary to reduce the dimensions of the integrated circuit's transistors. For example, it is expected that future integrated circuit transistors will be fabricated with effective channel lengths of one hundred nanometers or less.

Such small transistors often suffer from fringing fields and other short channel effects which degrade performance and diminish control over the transistor's operation. To reduce the short channel effects, a thinner gate dielectric often is used. However, the thin gate dielectric often results in excessive gate leakage current, which increases power and lowers the performance of the integrated circuit.

Hence, there is a need for a transistor that has small physical dimensions but does not suffer from short channel effects or excessive gate leakage current.

## Brief Description of the Drawings

The specific objects and advantages of the present instant invention will become readily apparent to those skilled in the art from the following detailed description thereof taken in conjunction with the drawings in which:

FIG. 1 is a top view of a portion of an integrated circuit;

FIG. 2 shows a cross-sectional view of the integrated circuit at a processing step where a transistors gate dielectric is being fabricated; and

FIG. 3 shows a cross-sectional view of the integrated circuit at a later stage of fabrication.

## DETAILED DESCRIPTION OF THE DRAWINGS

In the figures, elements having the same reference numbers have similar functionality.

FIG. 1 is a top view of an integrated circuit 10, showing a transistor 12 formed on a semiconductor substrate 14. In the embodiment of FIG. 1, transistor 12 is an N-channel metal-oxide-semiconductor transistor. Transistor 12 includes a drain 16, a source 18 and a gate 20, which are coupled to other devices (not shown) of integrated circuit 10 with interconnect lines 22, 24 and 26, respectively.

Substrate 14 typically is formed from silicon. Alternatively, another semiconductor material may be used, such as gallium arsenide, germanium, and the like.

FIG. 2 is a cross-sectional view of integrated circuit 10 during a step of the fabrication of a dual layer gate dielectric 29 over a channel region 30 of transistor 12. Portions of substrate 14 are doped with an N-type impurity such as phosphorous or

arsenic to form drain 16 and source 18 as shown. The distance from drain 16 to source 18 typically is one hundred nanometers or less.

Gate dielectric 29 includes an amorphous layer 40 typically comprising silicon dioxide. Gate dielectric 29 further includes a crystalline layer 42 typically comprising strontium titanate ($SrTiO_3$). Here it should be noted that crystalline layer 42 is generally grown as a single crystal (monocrystalline) structure whereas amorphous layer 40 is generally referred to as a layer with no short or long range ordering.

Integrated circuit 10 is shown as placed in a chamber of a molecular beam epitaxial (MBE) reactor or similar apparatus. An atmosphere of gaseous titanium (Ti) atoms 32, strontium (Sr) atoms 34 and oxygen ($O_2$) molecules 36 is formed in the MBE reactor at an ambient temperature between 400 and 600 degrees Celsius and a pressure of between $10^{-9}$ and $10^{-5}$ millibars. A titanium cell (not shown) is locally heated to a temperature of about 1,750 degrees Celsius to vaporize the titanium to produce titanium atoms 32. A strontium cell (not shown) is heated to a temperature of about 450 degrees Celsius to produce strontium atoms 34. Strontium atoms 34 and titanium atoms 32 are generated in approximately stoichiometric proportions for forming crystalline strontium titanate. Oxygen molecules 36 are supplied in an excess of stoichiometric proportions by operating an oxygen source (not shown) at an overpressure of approximately $10^{-6}$ millibars.

The titanium atoms 32, strontium atoms 34 and oxygen molecules 36 react to form strontium titanate molecules 46. Under the described conditions, strontium titanate molecules grow in a crystalline fashion to form crystalline layer 42. A first molecular layer of crystalline layer 42 is shown in FIG. 2 as open circles connected with lines to represent crystallized strontium titanate molecules 46 and their intermolecular binding forces. Further reaction leads to additional molecular layers of strontium titanate being crystallized over the first molecular layer.

Oxygen molecules 36 are present in greater than stoichiometric proportions, so that excess oxygen is available to diffuse through crystalline layer 42 to react with

silicon atoms of substrate 14. The reaction produces silicon dioxide molecules 44, represented in FIG. 2 as squares, overlying the surface of substrate 14. Silicon dioxide molecules 44 grow in a non-crystalline fashion to form amorphous layer 40.

As a feature of the present invention, amorphous layer 40 is grown while crystalline layer 42 is being grown. Hence, only one thermal processing step is needed to form both amorphous layer 40 and crystalline layer 42, thereby achieving a low fabrication cost of integrated circuit 10. In addition, the formation of amorphous layer 40 between substrate 14 and crystalline layer 42 results in a high quality for gate dielectric 29 by operating as a transition material to absorb lattice stress between substrate 14 and crystalline layer 42.

FIG. 3 shows a cross-sectional view of integrated circuit 10 at a later processing step than the step described in FIG. 2. Transistor 12 includes drain 16 and source 18 formed in substrate 14. Gate dielectric 29 includes amorphous layer 40 and crystalline layer 42. A gate electrode 26 is disposed over gate dielectric 29 to produce a gate capacitance between gate electrode 26 and substrate 14 which is charged by a control signal VIN applied to gate electrode 26.

Amorphous layer 40 typically comprises silicon dioxide grown to a thickness of ten angstroms. Depending on the application, the thickness of amorphous layer 40 typically ranges between eight and thirty angstroms. Amorphous layer 40 typically has a relative permittivity, i.e., a dielectric constant, of approximately 3.9. Alternatively, amorphous layer 40 may comprise another material such as silicon nitride, strontium silicate, or the like. Amorphous layer 40 preferably has a dielectric constant less than about ten.

Crystalline layer 42 is formed with strontium titanate typically grown to a thickness of approximately fifty angstroms. Depending on the application, the thickness of crystalline layer 42 typically ranges from thirty to one hundred angstroms. In the embodiment of FIG. 3, crystalline layer 42 has a dielectric constant of approximately two hundred, with a range between thirty and three hundred. The

dielectric constant of crystalline layer 42 preferably is greater than the dielectric constant of amorphous layer 40.

Note that crystalline layer 42 may be formed with materials other than strontium titanate. For example, Perovskite materials formed by combining alkaline earth metals, e.g., lanthanum, barium, strontium, or magnesium, with transition metals, e.g., titanium, aluminum, or zirconium, can be used to form crystalline layer 42.

In operation, control signal $V_{IN}$ is applied to gate 26 to charge the gate capacitance of transistor 12. An electric field 60 is produced across gate dielectric 29 which modifies the conductivity of substrate 14 and produces a conduction channel 52 in substrate 14 between source 18 and drain 16. In response to electric field 60, a polarizing field 62 is produced within crystalline layer 42 and a polarizing field 64 is produced within amorphous layer 40. Since the dielectric constant of crystalline layer 42 is greater than the dielectric constant of amorphous layer 40, polarizing field 64 is greater than polarizing field 62.

The gate capacitance of transistor 12 depends on the thickness and effective permittivity of gate dielectric 29. As a consequence of the present invention, gate dielectric 29 can be grown to a greater thickness than transistors having low permittivity gate dielectrics. The increased thickness virtually eliminates excessive gate leakage of transistor 12 to improve the performance of integrated circuit 10. In addition, the low relative permittivity of amorphous layer 40 reduces fringing fields of transistor 12 due to control signal $V_{IN}$, thereby avoiding short channel effects and improving control over the threshold voltage of transistor 12.

Hence, it should be appreciated that the present invention provides a transistor which can be scaled to dimensions less than one hundred nanometers while maintaining high performance operation and a low fabrication cost. A dual layer gate dielectric is formed over a semiconductor substrate to include a first layer formed with an amorphous material and a second layer formed with a crystalline material. The amorphous material provides a transition for a lattice mismatch between the substrate

and the monocrystalline material, and has a low dielectric constant to reduce fringing fields. The monocrystalline material has a high dielectric constant, in part due to its crystalline nature, and is formed to a thickness adequate to eliminate excessive gate leakage.

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While we have shown and described specific embodiments of the present invention, further modifications and improvements will occur to those skilled in the art. We desire it to be understood, therefore, that this invention is not limited to the particular forms shown and we intend in the appended claims to cover all modifications
10 that do not depart from the spirit and scope of this invention.